Laboratory 3 Report
Layout Drafting and Verification in Virtuoso

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1 Introduction

The layout process is a fundamental stage to designing any modern day electronic systems and integrated circuit. This laboratory activity will explore the critical process of taking a schematic level design and translating it to a layout that can be physically realized. The end goal will be to design, implement, and simulate the layout of a Common-source Amplifier.

2 Common-source Amplifier

2.1 Schematic Entry

The transistor level design for the Common-source Amplifier was entered into Virtuoso using schematic entry, as seen in Fig. 1. Then a symbol was made for the amplifier as seen in Fig. 2. All the component values can be read off the symbol or schematic, and are exactly as stated in the laboratory manual document.

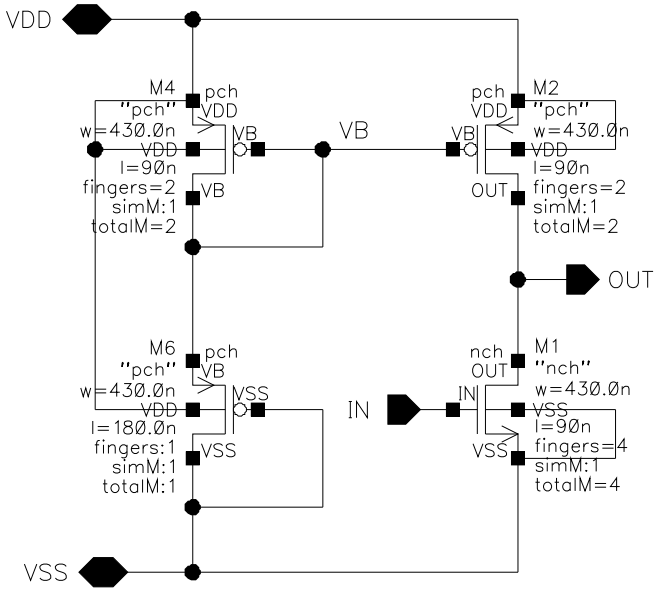

Figure 1: Schematic of the Common-source amplifier

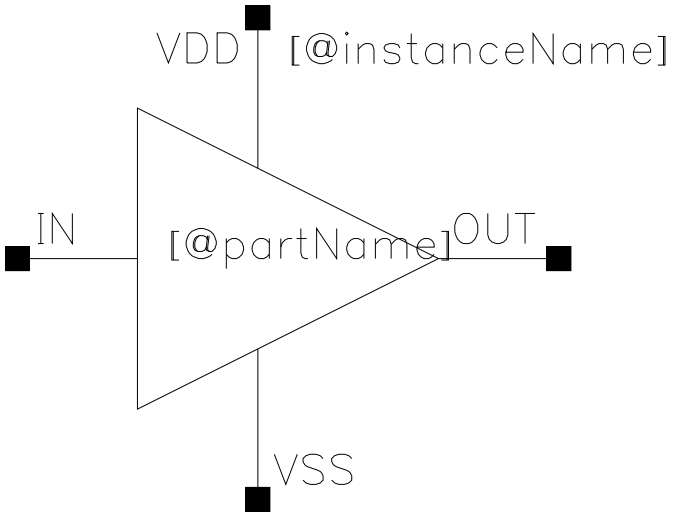

Figure 2: Symbol of the Common-source Amplifier

2.2 Test Bench

A new schematic was entered to act as a test bench for a simulation of the amplifier. All the component values can be seen in Fig. 1, Fig. 2, or from the provided test bench in the laboratory manual. Any other changes can be read off the schematic in Fig. 3.

2.3 Pre-layout Simulation

At this stage in the design a simulation was run to validate the schematic and the test bench. The final results of this can be seen along with the Post-layout simulation in Fig. 8. The simulation

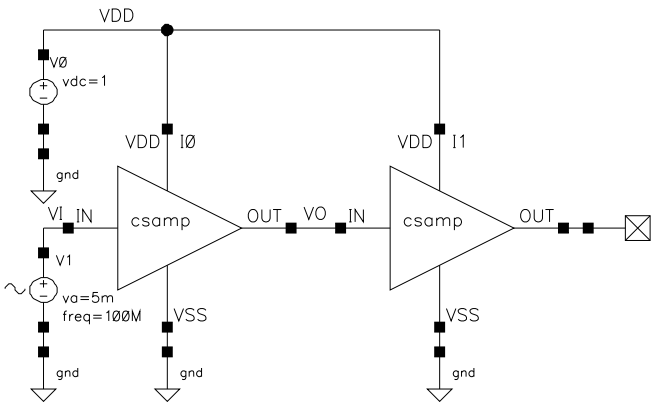

Figure 3: Schematic view of test bench for the Common-source Amplifier

conditions are also the same as the Post-layout simulation.

2.4 Layout

The next stage was to draw the equivalent layout and minimize the area of the amplifier. The layout provided within the laboratory manual was replicated as closely as possible. The final layout can be seen in Fig. 4. This design is heavily influenced by the Design Rule Check, as there were many cycles of modifying the layout, re-running the DRC, and fixing new errors that arose. It is worth noting in the final layout, both of the two-finger PMOS transistors are overlaid and share a source to minimize area.

2.5 Design Rule Check

The Calibre DRC was a very important part of the layout design. It is an extremely useful tool to ensure all the requirements of the TSMC 65nm process node are kept. After many hours of work it was a triumphant success to see the the DRC output in Fig. 5. It is worth noting the output is not error free, but the DN and R errors can be ignored as per the laboratory manual. After discussing with TA Masoud the ESD warning can also be ignored.

2.6 Layout Versus Schematic

It would be an understatement to say that it is critical to have the correct pin configuration for the LVS to pass. Ensuring the pins were correctly configured proved to be challenging but TA Masoud was very helpful in this regard. The passing LVS can be seen in Fig. 6.

2.7 Parasitics Extraction

The next step was to run the Parasitics Extraction as the penultimate step before the post-layout simulation can be run. The result seen in Fig. 7 was a new Calibre cell view that had the transistors, pins, and a very long array of capacitors and resistors to model the parasitics of the layout.

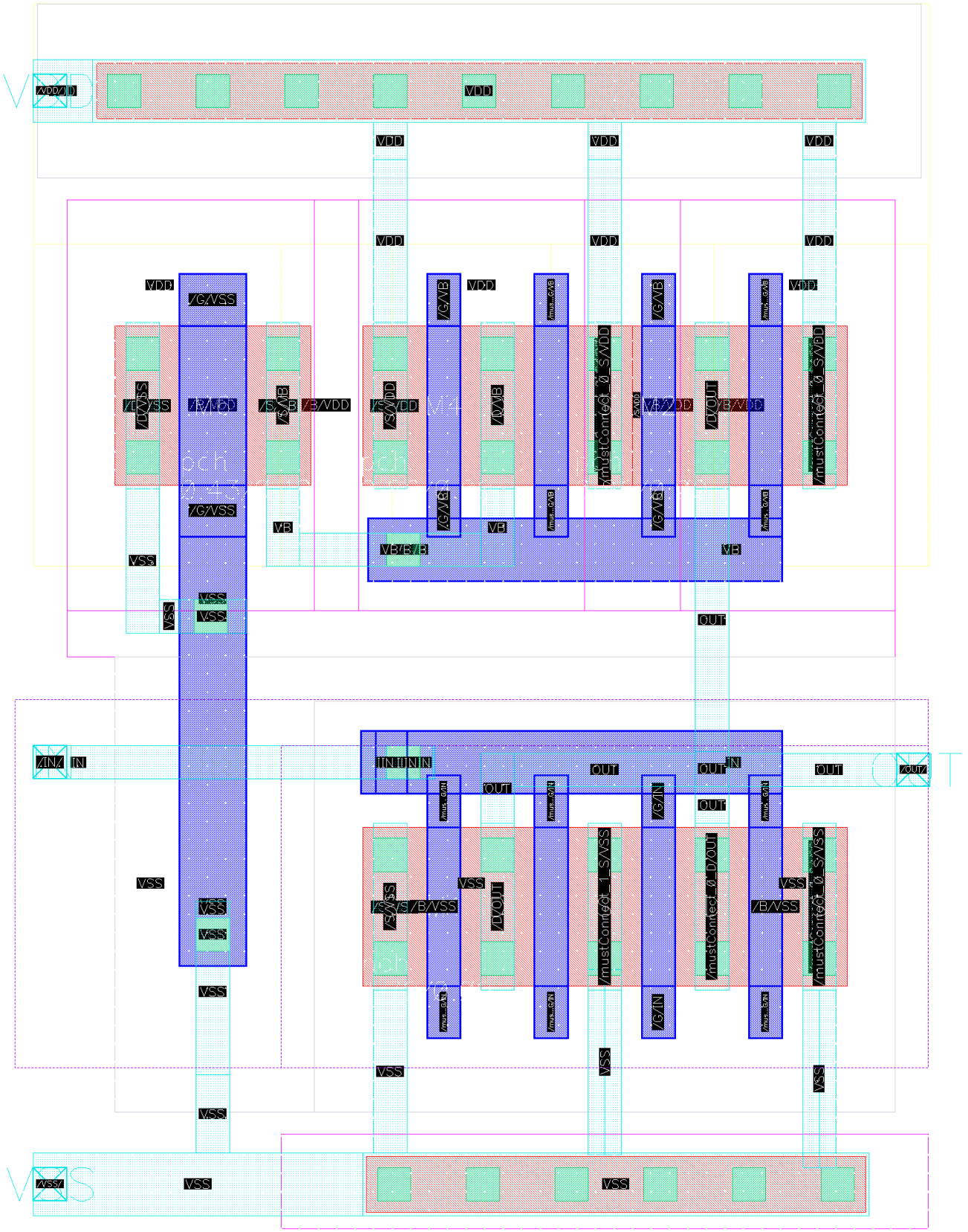

Figure 4: The final layout of the Common-source Amplifier

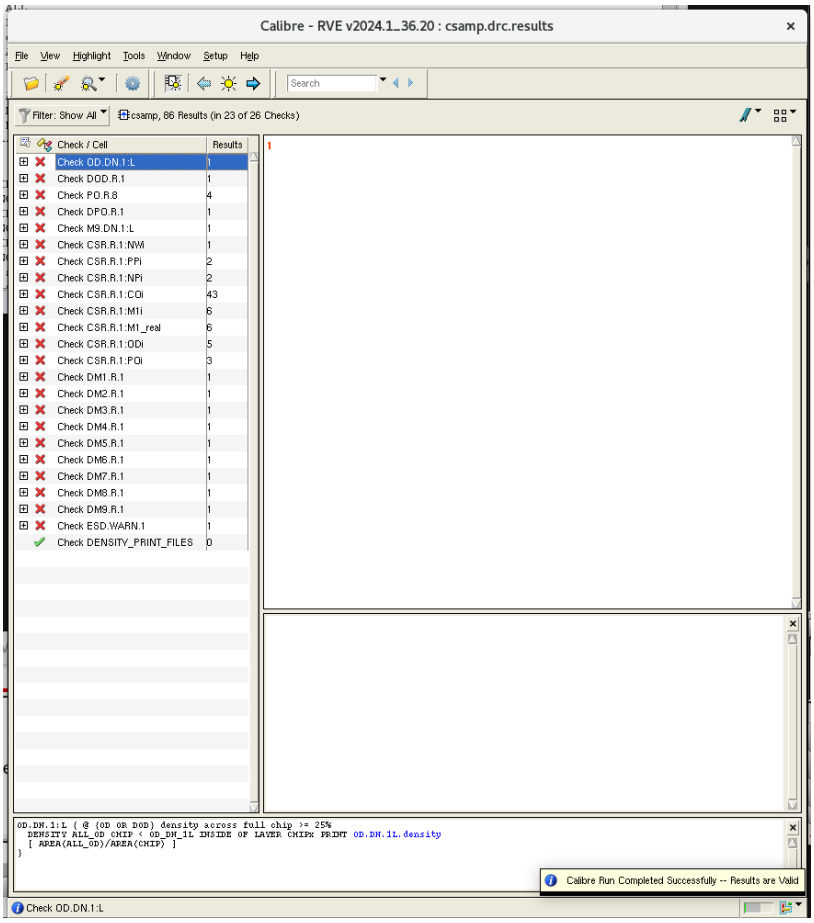

Figure 5: The DRC results

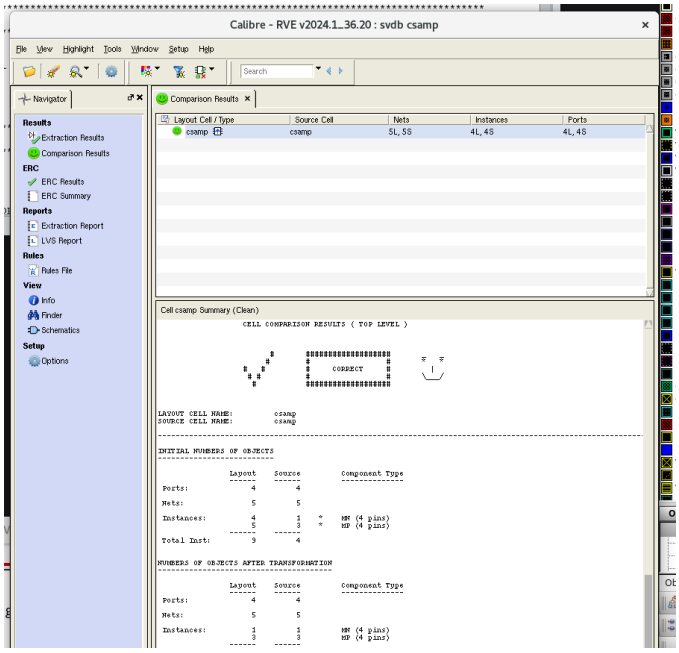

Figure 6: The LVS results

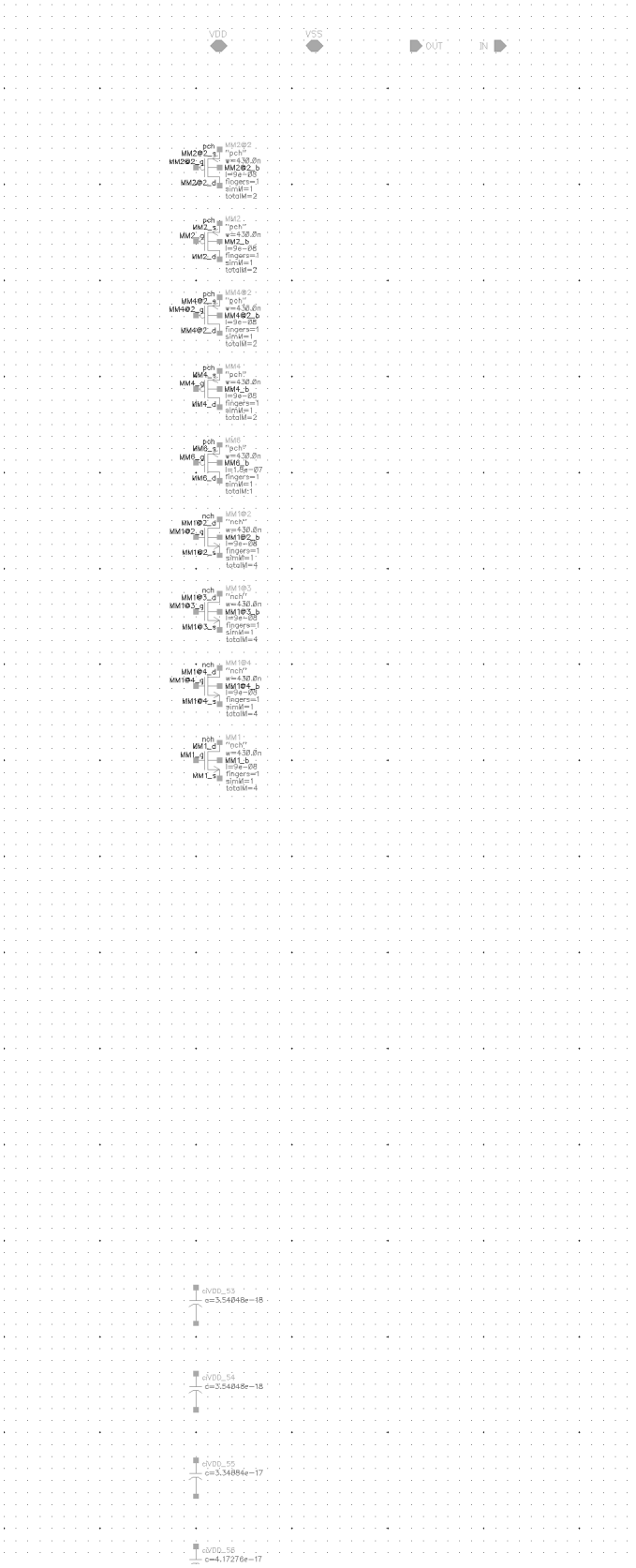

Figure 7: Calibre schematic of the PEX results

2.8 Post-layout Simulation

The final plot of the amplifier simulation can be seen in Fig. 8. In the final waveform one can see the input signal, the output signal from the schematic, and the output signal from the layout. In the simulation VDD supply voltage was kept a 1V, and VSS was grounded. The input VI is exactly as specified in the laboratory manual. This simulation used transient analysis with a fixed time of $30ns$, an AC analysis with a sweep from 100 kHz to 100 GHz, and a DC analysis with a sweep from 0 V to 1 V. All simulations were at ambient temperature with no corner cases for the TSMC 65nm process. To produce the plots seen in Fig. 8 first the pre-layout simulation was run as is standard in ADE. Then ADE was switched to append mode, and the simulation was rerun using the calibre cell view to take the parasitics of the layout into consideration. Both can be seen on the same plot and additional details further demonstrating insight into the subject matter can be found in Section 3.1 **Further Discussion of Simulation Results**.

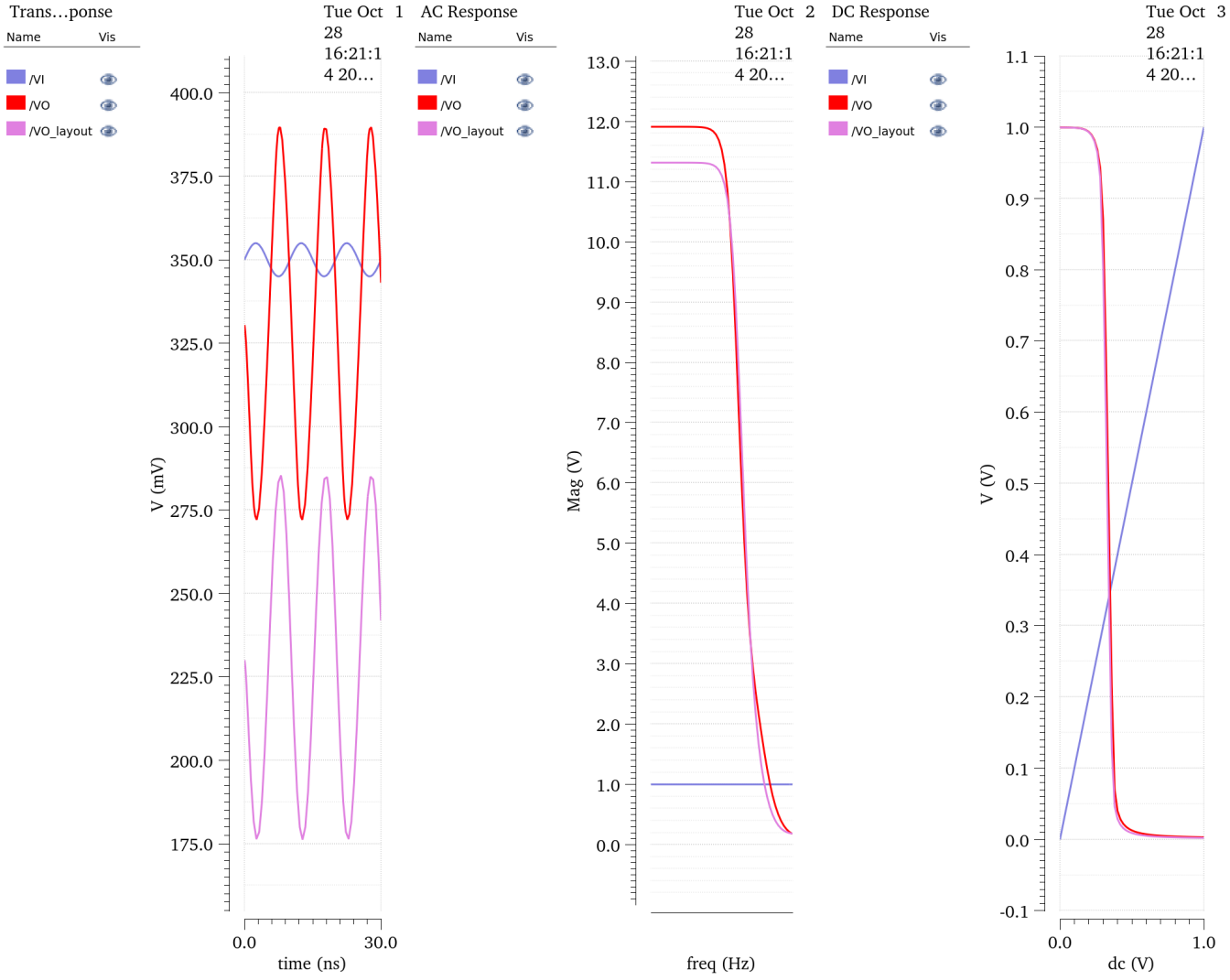

Figure 8: Post-layout simulation plot appended to the pre-layout simulation

3 Observations and Conclusions

3.1 Further Discussion of Simulation Results

As seen in Fig. 8 the response for the layout of the amplifier from Fig. 4 does not conform to the provided Figure 25 in the laboratory manual. From a discussion with TA Masoud despite the strange result it is still entirely valid and correct. The proposed explanation seems to be that there is a greater amount of parasitics effecting the layout than anticipated. This comes down to the intricacies and specifics of the layout. One could of course reduce the parasitics further by increasing the spacing of certain components, but this would also increase the area.

Comparing the two plots one can also see that the pre-layout schematic output exactly follows Figure 25 in the laboratory manual. It it also worth noting the outputs appear to be 180 degrees out of phase with the input. In other words the Common-source Amplifier is an inverting design as expected from lecture, and laboratory exercise 1. Both the AC and AD signals look exactly like the expected results from Figure 25 in the laboratory manual.

3.2 Parting Thoughts

This laboratory activity again helped build a stronger understanding of the Cadence Virtuoso design tools and provided insight into the new subject matters of layout, DRC, LVS, and PEX. The obtained results were able to be explained based on the theory, and align with the expected behaviour of Common-source Amplifiers and the TSMC 65nm layout rules. Getting to use the layout editor was both a very frustrating and enjoyable process, and this laboratory activity proved to be quite fun.