Laboratory 1 Report
Schematic entry and circuit simulation in Virtuoso

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1 Introduction

Modern day electronic systems and integrated circuits (IC) rely heavily on transistors, specifically Metal Oxide Semiconductor Field Effect Transistors (MOSFET) using Complimentary Metal Oxide Semiconductor (CMOS) technology. MOSFETs are very versatile devices, and can be used as amplifiers, or switches. When assembled together they can make logic gates, and build large scale ICs. This laboratory was completed using the TSMC 65-nm CMOS technology. This laboratory is comprised of two experiments that teach the fundamentals of schematic entry and circuit simulation in Cadence Virtuoso. The first relates to simple n-type and p-type MOSFETs. The seconds relates to a Common-source amplifier making use of the two types of MOSFETs from the first experiment.

2 Experiment 1: NMOS and PMOS Transistors

2.1 Entry

The design for the NMOS and PMOS MOSFETs were entered into Virtuoso. The resulting schematics for the NMOS and PMOS can be seen in Fig. 1. All the component values can be read off the schematics.

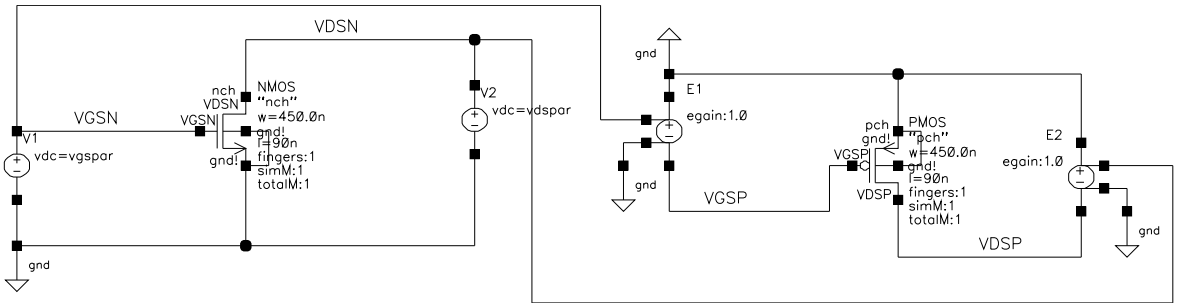

Figure 1: Schematic for NMOS and PMOS

2.2 Simulation & Analysis

A DC Simulation of the NMOS and PMOS transistors was performed. The resulting $I_D - V_{GS}$ and $I_D - V_{DS}$ plots along with derivative functions of the simulation can be seen in Fig. 2, Fig. 3, and Fig. 4. To collect g_m, r_{DS}, and V_{th} this simulation used DC analysis for the TSMC 65nm process. All simulation was at ambient temperature with no corner cases. To collect g_m, and r_{DS} 425 mV was applied to the voltage source not being swept for the simulation. It is important to remember that the intercept point minus $\frac{V_{DS}}{2}$ corresponds to V_{th}, where $V_{DS} = 10$mV for related simulations. It is also worth noting that the values for r_{DS} are the inverse of the intercept values read off the plots. The second round of simulations provided a value of $g_m = 258.2\mu S$ for NMOS with a 900nm width, and $g_m = 111.4\mu S$ for PMOS with a 900nm width. Also a value of $r_{DS} = 69.1k\Omega$ for NMOS with a 900nm width, and $r_{DS} = 107.1k\Omega$ for PMOS with a 900nm width. Lastly a value of $V_{th} = 365.9mV$ for NMOS with a 900nm width, and $V_{th} = 359.3mV$ for PMOS with a 900nm width. The values for MOSFETs with a 900nm width are listed directly without their plots as Masoud has instructed in the laboratory environment.

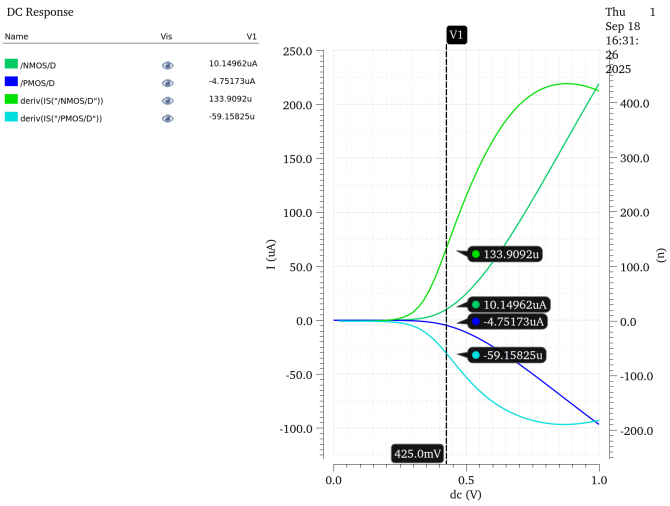

Figure 2: Value of $g_m = 133.9\mu S$ for NMOS and $g_m = 59.2\mu S$ for PMOS with a 450nm width

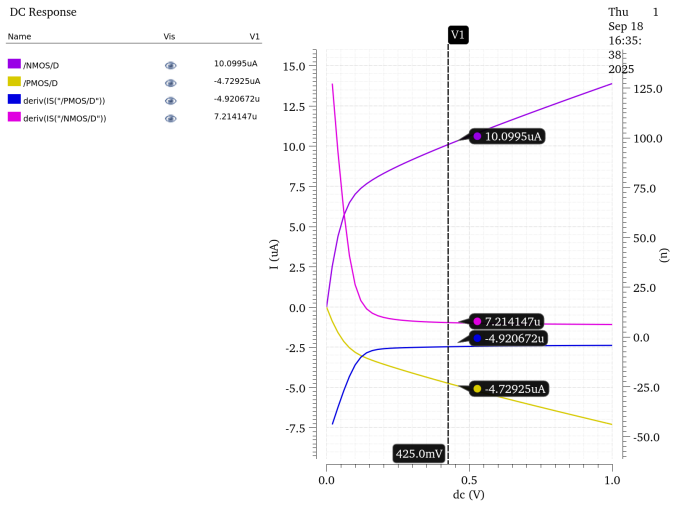

Figure 3: Value of $r_{DS} = 138.6k\Omega$ for NMOS, and $r_{DS} = 203.2k\Omega$ for PMOS with a 450nm width

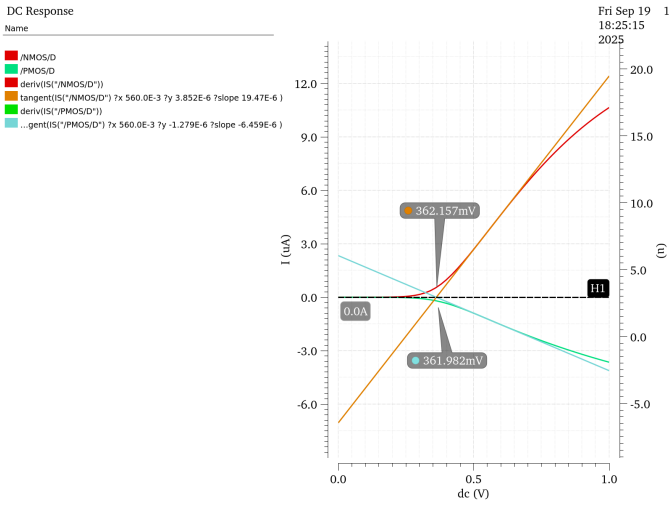

Figure 4: Value of $V_{th} = 357.2mV$ for NMOS, and $V_{th} = 357.0mV$ for PMOS with a 450nm width

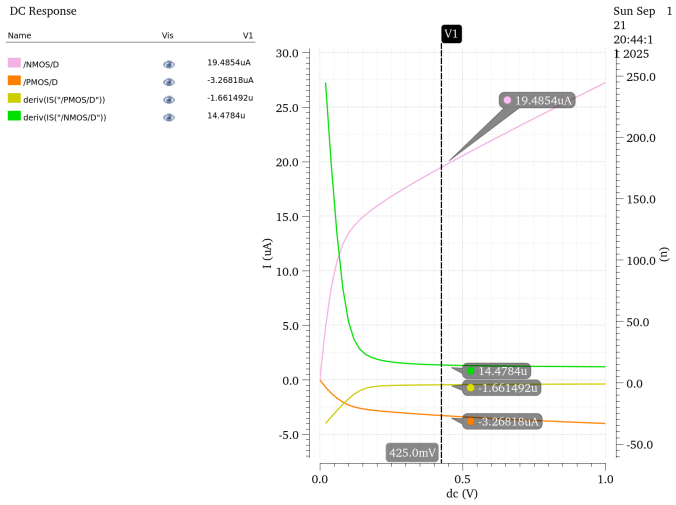

Figure 5: Value of $r_{DS} = 69.1k\Omega$ for NMOS width of 900nm, and $r_{DS} = 601.9k\Omega$ for a PMOS with a 450nm width and a length of 180nm

3 Experiment 2: Common-source Amplifier

3.1 Entry

The schematic for the Common-source Amplifier was entered into Virtuoso as seen in Fig. 6. Nearly all component values can be read off the schematics, except for the sinusoidal voltage source **V1** has an AC magnitude 1 volt, and a variable DC voltage **vindc**.

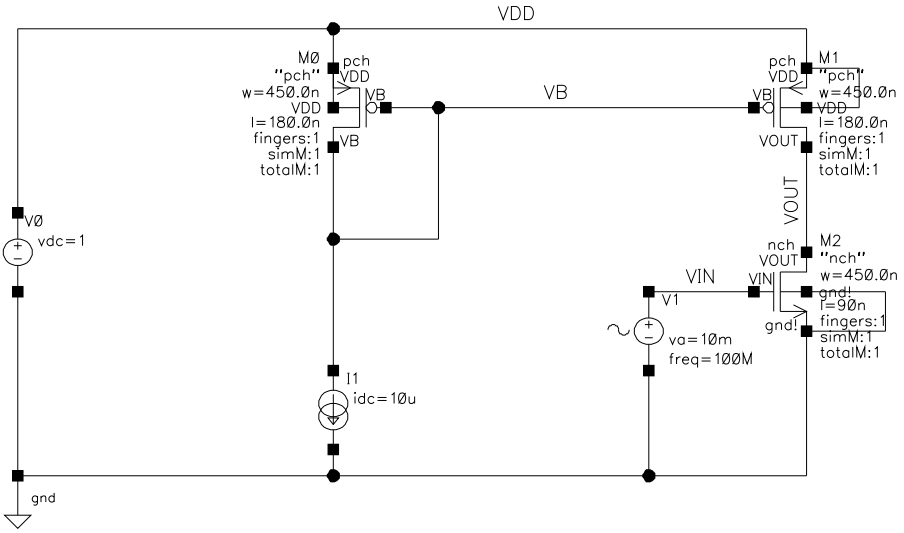

Figure 6: Schematic of the Common-source Amplifier

3.2 Analysis

The small signal model of common-source amplifier was drawn as seen in Fig. 7. As a result the voltage gain of the amplifier was calculated using the small-signal model as

$$A_v = \frac{V_{out}}{V_{in}} = -g_m(r_{DS_1} \;//\; r_{DS_2})$$

The values g_m and r_{DS_1} pertain to NMOS M_1, where r_{DS_2} pertains to PMOS M_2. To calculate the voltage gain of the amplifier using the bias current value and transistor sizes of Fig. 6 the values of g_m, r_{DS_1} are already known as seen in Fig. 2, and Fig. 3 respectively. A portion of Experiment 1 needed to be run again with a PMOS length of 180nm to match the current-mirror active load in the amplifier as seen in Fig. 5. Thus $A_v = -(133.9092\mu S) \cdot (138.6165k\Omega \;//\; 601.8687k\Omega) = -15.09$.

3.3 Simulation

Next the voltage gain was measured using transient and AC analysis. These simulation results can be compared with the calculated values above. A DC Simulation of the amplifier was also performed. The resulting plots of the simulation can be seen in Fig. 8. This simulation was at ambient temperature with no corner cases on the TSMC 65nm process. The supply voltage can be read of as VIN in Fig. 8. The resulting gain of the AC response can simply be read off the intercept in Fig. 8 since the input voltage is 1V, and gives a gain of $A_v = 13.74$. It is also possible to read the gain from the transient analysis.

$$A_v = \frac{569.01mV - 298.45mV}{415.03mV - 434.95mV} = -13.58$$

Insights into this subject matter, and comments on the results, can be found in Section 4.1 **Amplifier Gain Measurement Using Transient and AC Analysis**.

Then a simulation was performed to test the effect of the bias current. This simulation was at ambient temperature with no corner cases on the TSMC 65nm process. The supply voltage was a steady 1 V on VIN. To be able to see the maximum swing for each bias current the **vindc** parameter needed to be adjusted for every run. The required voltages were: $V_{GS5\mu} = 387.631mV, V_{GS10\mu} = 425mV, V_{GS15\mu} = 451.9901mV, V_{GS20\mu} = 473.1436mV$, A sample of a portion of results can be seen in Fig. 9, the rest of the plots are omitted by recommendation of Masoud to fit within the page limit. The small-signal voltage gain with the maximum swing for each value is a follows:

$$A_{V_{5\mu A}} = -14.67, A_{V_{10\mu A}} = -13.58, A_{V_{15\mu A}} = -12.39, A_{V_{20\mu A}} = -11.47$$

This result is justified by discussing g_m and r_{DS}. From the lecture notes is it know that:

$$g_m = \frac{\partial I_D}{\partial V_{GS}}, \qquad r_{DS} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1}$$

Using a modified formula for the gain we see

$$A_v = -g_m(r_{DS}) = \left(\frac{\partial I_D}{\partial V_{GS}}\right)\left(\frac{\partial V_{DS}}{\partial I_D}\right)$$

The partial derivative ∂I_D cancels out leaving a gain that is dependant on V_{DS} in the numerator and V_{GS} in the denominator. Since V_{DS} is not changed in this experiment it is clear now to see that as V_{GS} increases the resulting gain will decrease since V_{GS} is in the denominator. This justifies why the gain decreases as the bias current is raised, since the V_{GS} must also change for maximum swing of the gain.

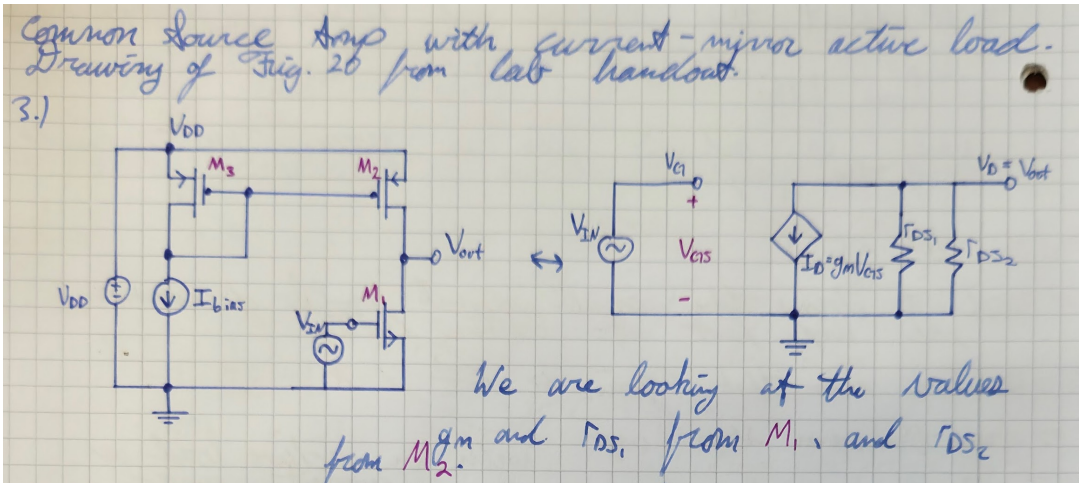

Figure 7: Circuit diagram of the Common-source Amplifier, and the small signal model.

The last portion of this experiment was an attempt to increase the gain of the amplifier by 20%. A final simulation was made under similar conditions to above. This time the width of the

transistor M1 was set as parameter and swept from 200nm to 600nm to see if any increases in gain could be made. The results are shown in Fig. 10. Insights into this subject matter, and comments on the results, can be found in Section 4.2 **Amplifier Gain Increase**.

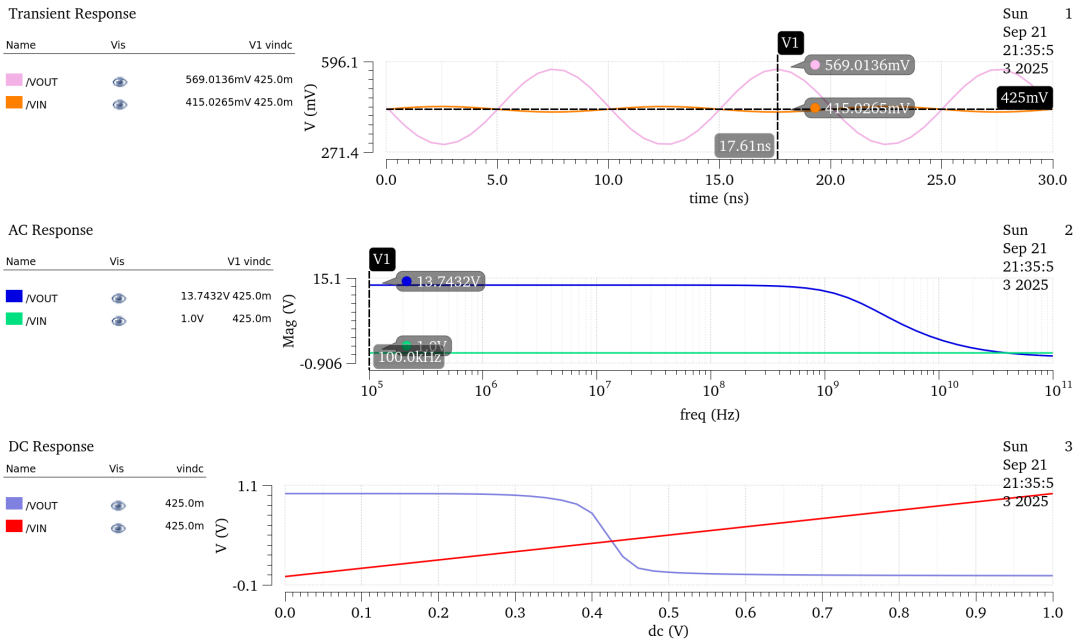

Figure 8: Transient, AC, and DC analysis of the Common-source Amplifier

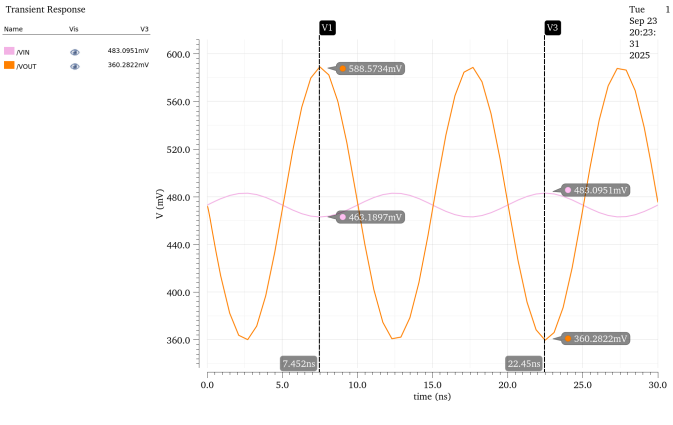

Figure 9: Transient response of the amplifier with $20\mu A$ of bias current and a **vindc** value of 473.1436mV

Figure 10: Parametric width simulation from 200nm to 600nm

4 Observations and Conclusions

4.1 Amplifier Gain Measurement Using Transient and AC Analysis

There are three values for the Common-source Amplifier Gain Measurement. Experimentally through simulation are gains of -13.58, and 13.74. While these values are not the same their magnitudes are close to each other. This can then be compared back to the gain $A_v = -15.09$ from the small signal analysis, which is approximately 10% off from the value of -13.58. There is naturally an error introduced because the small signal model is not perfect and neglects certain portions of the amplifiers operation such as body effects. This shows that the small signal analysis provides a reasonable approximation of the amplifier but does not quite align with the sophisticated Spectre simulation in Virtuoso.

4.2 Amplifier Gain Increase

As seen in Fig. 10 regardless of increasing or decreaing the widther there is no result with a gain greater than 13.74. Thus it does not seem possible to increase the gain by 20%, and not possible to calculate the new value of W as shown in the simulations. It is proposed that one may use amplifier chaining to increase the gain. Having a multi-stage amplifier allows for the output of the first amplifier to be the input of the second amplifier, thus resulting in a net gain that is greater than using just a single amplifier.

4.3 Parting Thoughts

This laboratory activity helped build a stronger understanding of the Cadence Virtuoso design tools and provided insight into the subject matter of PMOS, NMOS, and Common-source Amplifier operation. The obtained results were able to be explained based on the theory. It will be important to remember the fundamental principals of PMOS, NMOS, and Common-source Amplifier operation. It will also be critical to retain the skills of small signal analysis from this laboratory activity.